REMARKS

This Amendment responds to the Office Action dated August 12, 2002 in which the Examiner rejected claims 7, 9-10, 12 and 15-16 under 35 U.S.C. §102(e) and objected to claims 8, 11, 13-14 and 17 as being dependent upon a rejected base claim but would be allowable if rewritten in independent form.

As indicated above, new claim 18 has been added.

Claim 7 claims a method of manufacturing electronic devices obtained by equipping with electronic component chips on a printed circuit board. The method comprises the steps of: first, supplying a plurality of electronic component chips in an aligned relationship and then cleaning outer surfaces of the electronic component chip.

Through the method of the claimed invention a) supplying a plurality of electronic component chips that are to be mounted on a printed circuit and b) cleaning the outer surfaces of the chips, as claimed in claim 7, the claimed invention provides a method of manufacturing electronic devices in which reliable electrical connection is provided. The prior art does not show, teach or suggest the invention as claimed in claim 7.

Claim 7, 9, 12 and 15 were rejected under 35 U.S.C. §102(e) as being anticipated by *Ishikawa et al.* (U.S. Patent No. 6,257,966).

Applicants respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. §102(e). The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, Applicants respectfully request the Examiner withdraws the rejection to the claims and allows the claims to issue.

Ishikawa et al. appears to disclose a wafer surface machining apparatus, and more particularly a wafer surface machining apparatus for grinding the reverse surface of a semiconductor wafer in a semiconductor wafer manufacturing process. (col. 1, lines 5-9) At the alignment stage 16, the wafer 26 transferred from the cassette 24 is aligned to a predetermined position. The aligned wafer 26 is held on the suction pads 35 of the transfer robot 28. Then, the wafer 26 is transferred to a chuck table 48, and it is held at a preset position on the chuck table 48. The chuck table 52 is located at the rough grinding stage 18, and the wafer 26 held on the chuck table 52 is roughly ground. The chuck table 54 is located at the finish grinding stage 20, and the wafer 26 held on the chuck table 54 is finish-ground. (col. 4, lines 37-51) On completion of the finish grinding at the finish grinding stage 20, the cup-shaped grindstone 64 moves away from the wafer 26, and the wafer 26 is transferred to the position of the chuck table 48 in FIG. 1 due to the turn of the turn table 50 in the direction of the arrow C. The wafer 26 is held on a suction disc 68 provided at the end of a moving part or a transfer arm 66. The suction disc 68 has a disc-shaped porous suction surface 68A, which has substantially the same diameter as the wafer 26. Then, the wafer 26 is transferred to the cleaning stage 22 due to the turn of the transfer arm 66 in the direction of an arrow D in FIG. 1. (col. 5, lines 18-28) The wafer 26 is cleaned at the cleaning stage 22, and it is stored on a predetermined shelf of the predetermined cassette 24. This completes the wafer processing procedure of the surface machining apparatus 10. (col. 5, lines 59-63) As shown in FIGS. 1 and 2, a spin cleaner 72 as the first cleaning device is disposed in a sink 70, and a brush scrubber 74 as the second cleaning device is disposed between the spin cleaner 72 and the turn table 50. As

shown in FIG. 6, the spin cleaner 72 has a suction pad 120 of substantially the same diameter as the wafer 26. A spindle 124 of a motor 122 connects to the reverse surface of the suction pad 120. A nozzle 126 is provided above the suction pad 120, and cleaning water is supplied through the nozzle 126. The spin cleaner 72 jets the cleaning water against the reverse surface 26A of the wafer 26 through the nozzle 126 while rotating the wafer 26 held on the suction pad 120. This eliminates the sludge, etc. adhered to the reverse surface 26A of the wafer 26. (col. 8, lines 1-10)

Thus, *Ishikawa et al.* has a U.S. filing date which is subsequent to the Japanese priority date of the present application which is September 28, 1998. Therefore, Applicants respectfully point out that *Ishikawa et al.* is not a proper reference.

Additionally, *Ishikawa et al.* is merely directed to cleaning a wafer surface. Nothing in *Ishikawa et al.* shows, teaches or suggests a method of manufacturing electronic devices in which electronic component chips are provided on a printed circuit board as claimed in claim 7 and new claim 18. Rather, *Ishikawa et al.* is merely directed to cleaning surfaces of wafers.

Additionally, since *Ishikawa et al.* is merely directed to cleaning the surface of a wafer, nothing in *Ishikawa et al.* shows, teaches or suggests supplying a plurality of a electronic component chips in an aligned relationship as claimed in claims 1 and 18. Additionally, *Ishikawa et al.* does not show, teach or suggest that the aligned electronic component chips are taken out one at a time from a chute portion connected to a buffer portion as claimed in claim 18. Finally, nothing in *Ishikawa et al.* shows, teaches or

suggests cleaning external electrodes of the electronic component chips as claimed in claim 18. Rather, *Ishikawa et al.* merely discloses cleaning wafers.

Since *Ishikawa et al.* is not a proper reference and is not directed to a method of manufacturing electronic devices in which the electronic component chips are provided on a printed circuit board for supplying the electronic component chips in an aligned relationship as claimed in claim 7, it is respectfully requested that the Examiner withdraws the rejection to claim 7 under 35 U.S.C. §102(e) and allows new claim 18.

Claims 9, 12 and 15 depend from claim 7 and recite additional features. It is respectfully submitted that claims 9, 12 and 15 would not have been anticipated by *Ishikawa et al.* within the meaning of 35 U.S.C. §102(e) at least for the reasons as set forth above. Therefore, it is respectfully requested that the Examiner withdraws the rejection to claims 9, 12 and 15 under 35 U.S.C. §102(e).

Claims 7, 9-10, 12 and 15-16 were rejected under 35 U.S.C. §102(e) as being anticipated by *White* (U.S. Patent No. 6,241,583).

Applicants respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. §102(e). The claims have been reviewed in light of the Office Action, and for reasons which will be set forth, it is respectfully requested that the Examiner withdraws the rejection to the claims and allows the claims to issue.

White appears to disclose apparatus and methods for chemical mechanical polishing a substrate, and more particularly to such apparatus and methods using a moving polishing sheet. An integrated circuit is typically formed on a substrate by the sequential deposition of conductive, semiconductive or insulative layers on a silicon wafer. One fabrication step

involves depositing a filler layer over a patterned stop layer, and planarizing the filler layer until the stop layer is exposed. For example, trenches or holes in an insulative layer may be filled with a conductive layer. After planarization, the portions of the conductive layer remaining between the raised pattern of the insulative layer form vias, plugs and lines that provide conductive paths between thin film circuits on the substrate. Chemical mechanical polishing (CMP) is one accepted method of planarization. (col. 1, lines 12-28) Referring to FIGS. 1 and 2, one or more substrates 10 will be polished by a chemical mechanical polishing apparatus 20. Polishing apparatus 20 includes a machine base 22 with a table top 23 that supports a series of polishing stations, including a first polishing station 25a, a second polishing station 25b, and a final polishing station 25c, and a transfer station 27. Transfer station 27 serves multiple functions, including receiving individual substrates 10 from a loading apparatus (not shown), washing the substrates, loading the substrates into carrier heads, receiving the substrates from the carrier heads, washing the substrates again, and finally, transferring the substrates back to the loading apparatus. Each polishing station includes a rotatable platen. At least one of the polishing stations, such as first station 25a, includes a polishing cartridge 102 mounted to a rotatable, rectangular platen 100. The polishing cartridge 102 includes a linearly advanceable sheet or belt of fixed-abrasive polishing material. (col. 5, lines 36-56) Each polishing station 25a, 25b and 25c also includes a combined slurry/rinse arm 52 that projects over the associated polishing surface. Each slurry/rinse arm 52 may include two or more slurry supply tubes to provide a polishing liquid, slurry, or cleaning liquid to the surface of the polishing pad. (col. 6, lines 1-6)

Thus, Applicants respectfully again point out that the Japanese priority date of the present application of September 28, 1998 is prior to the U.S. filing date of *White*. Therefore, *White* is not a proper reference.

Additionally, *White* merely discloses planarizing a substrate using chemical mechanical polishing and a device therefore. Thus nothing in *White* shows, teaches or suggests electronic component chips provided on a printed circuit board as claimed in claim 7 and new claim 18. Rather, *White* is merely directed to polishing or planarizing a substrate.

Furthermore, *White* merely discloses a chemical mechanical polishing apparatus to contact a surface of a substrate during polishing. Nothing in *White* shows, teaches or suggest a) supplying a plurality of electronic component chips in an aligned relationship as claimed in claim 7 and 18, b) that the aligned electronic chip components are taken out one at a time from a chute portion connected to a buffer portion as claimed in claim 18, or c) cleaning external electrodes of the electronic component chips or cleaning outer surface of the electronic component chips as claimed in claims 7 and 18. Rather, *White* merely discloses chemical mechanical polishing in order to planarize (i.e. no cleaning is shown, taught or suggested by *White*).

Since nothing in *White* shows, teaches or suggests electronic component chips for a printed circuit board or cleaning of the chips as claimed in claim 7, it is respectfully requested that the Examiner withdraws the rejection to claim 7 under 35 U.S.C. §102(e) and allows new claim 18.

Claims 9-10, 12 and 15-16 depend from claim 7 and recite additional features. It is respectfully submitted that claims 9-10, 12 and 15-16 would not have been anticipated by *White* within the meaning of 35 U.S.C. §102(e) at least for the reasons as set forth above. Therefore, it is respectfully requested that the Examiner withdraws the rejection to claims 9-10, 12 and 15-16.

Since objected to claims 8, 11, 13-14 and 17 depend from allowable claims, it is respectfully requested that the Examiner withdraws the objection thereto.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason Examiner feels that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, Applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

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